Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A semiconductor package comprising:

a die pad;

a die mounted on the die pad and having an upper surface and a lower surface, the lower surface facing the die pad;

a plurality of outer leads electrically connected to electrodes of the die by bonding wires, respectively; and

a sealing member sealing therein the die, the bonding wires, parts of the outer leads and a part of the die pad, and having an [[upper]] uppermost surface ~~on the side~~ over the upper surface of the die and a lower surface under the lower surface of the die ~~on the side of the die pad~~;

wherein the outer leads extend at least from a plane including the lower surface of the sealing member to beyond that of the uppermost surface of the sealing member, each of the outer leads comprising an upper electrical connecting surface located above the uppermost surface of the sealing member, and a lower electrical connecting surface located at the lower surface of the sealing member ~~have upper electrical connecting surfaces on the side of the upper surface of the sealing member, and lower electrical connecting surfaces on the side of the lower surface of the sealing member, respectively, and the outer leads extend at least from a plane including the lower surface of the sealing member to beyond that of the upper surface of the sealing member~~.

2. (Currently Amended) The semiconductor package according to claim 1, wherein the upper electrical connecting surfaces of the outer leads ~~formed on the side of the upper surface of the sealing member~~ lie outside ~~a projection region of~~ an area over the [[upper]] uppermost surface of the sealing member.

3. (Currently Amended) The semiconductor package according to claim 1, wherein the sealing member has four sides surrounded by~~, and~~ the outer leads ~~are formed on the four sides of the sealing member~~.

4. (Original) The semiconductor package according to claims 1, wherein the outer leads are formed in an L-shape.

5. (Currently Amended) A semiconductor device comprising:

~~a printed wiring board; and~~

a plurality of semiconductor packages[[,]] arranged to be stacked up on [[the]] a printed wiring board with outer leads included therein; wherein each of the plurality of semiconductor packages comprises,

a die pad;

a die mounted on the die pad and having an upper surface and a lower surface, the lower surface facing the die pad;

the outer leads electrically connected to electrodes of the die by bonding wires, respectively; and

a sealing member sealing therein the die, the bonding wires, parts of the outer leads and a part of the die pad, and having an [[upper]] uppermost surface ~~on the side~~ over the upper surface of the die and a lower surface under the lower surface of the die ~~on the side of the die pad~~;

wherein the outer leads extend at least from a plane including the lower surface of the sealing member to beyond that of the uppermost surface of the sealing member, each of the outer leads comprising an upper electrical connecting surface located above the uppermost surface of the sealing member, and a lower electrical connecting surface located at the lower surface of the sealing member ~~have upper electrical connecting surfaces on the side of the upper surface of the sealing member, and lower electrical connecting surfaces on the side of the lower surface of the sealing member, respectively, and the outer leads have a height from a plane including the lower surface of the sealing member greater than that of the upper surface of the sealing member from the same plane~~.

6. (Currently Amended) The semiconductor device according to claim 5, wherein the upper electrical connecting surfaces of the outer leads ~~formed on the side of the upper surface of the sealing member~~ lie outside ~~a projection region of~~ an area over the [[upper]] uppermost surface of the sealing member.

7. (Currently Amended) The semiconductor device according to claim 5, wherein the sealing member has four sides surrounded by~~, and~~ the outer leads ~~are formed on the four sides of the sealing member~~.

8. (Original) The semiconductor device according to claims 5, wherein the outer leads are formed in an L-shape.

9. (Currently Amended) A semiconductor device comprising:

~~a printed wiring board; and~~

a plurality of semiconductor packages arranged to be mounted on [[the]] a printed wiring board, each semiconductor package having an upper surface of a sealing member thereof facing the printed wiring board and outer leads thereof connected to electrodes formed on the printed wiring board; wherein each of the plurality of semiconductor packages comprises,

a die pad;

a die mounted on the die pad and having an upper surface and a lower surface, the lower surface facing the die pad;

the outer leads electrically connected to electrodes of the die by bonding wires, respectively; and

the sealing member sealing therein the die, the bonding wires, parts of the outer leads and a part of the die pad, and having the upper surface ~~on the side~~ over the upper surface of the die and a lower surface under the lower surface of the die ~~on the side of the die pad~~;

wherein the outer leads have a height from a plane including the lower surface of the sealing member greater than that of the upper surface of the sealing member from the same plane, each of the outer leads comprising an upper electrical connecting surface located above the upper surface of the sealing member, and a lower electrical connecting surface located at the lower surface of the sealing member ~~have upper electrical connecting surfaces on the side of the~~

~~upper surface of the sealing member, and lower electrical connecting surfaces on the side of the lower surface of the sealing member, respectively, and the outer leads have a height from a plane including the lower surface of the sealing member greater than that of the upper surface of the sealing member from the same plane~~.

10. (Currently Amended) The semiconductor device according to claim 9, wherein the upper electrical connecting surfaces of the outer leads ~~formed on the side of the upper surface of the sealing member~~ lie outside ~~a projection region of~~ an area over the upper surface of the sealing member.

11. (Currently Amended) The semiconductor device according to claim 9, wherein the sealing member has four sides surrounded by~~, and~~ the outer leads ~~are formed on the four sides of the sealing member~~.

12. (Original) The semiconductor device according to claims 9, wherein the outer leads are formed in an L-shape.

13. (Currently Amended) The semiconductor device according to claim 9, further comprising a cooling fin arranged to be provided on an exposed surface of the die pad ~~wherein the die pad of the semiconductor package is provided on its exposed surface with a cooling fin~~.

14. (New) The semiconductor device according to claim 9, wherein each of the semiconductor package is arranged to be mounted on the printed wiring board such that the

upper surface of the sealing member faces that of another semiconductor package through the printed wiring board.

15. (New) A semiconductor device comprising:

a plurality of semiconductor packages arranged to be mounted on a printed wiring board, wherein each of the plurality of semiconductor packages comprises,

a die pad;

a die mounted on the die pad and having an upper surface and a lower surface, the lower surface facing the die pad;

a plurality of outer leads electrically connected to electrodes of the die by bonding wires, respectively; and

a sealing member sealing therein the die, the bonding wires, parts of the outer leads and a part of the die pad, and having an uppermost surface over the upper surface of the die and a lower surface under the lower surface of the die,

wherein the outer leads extend at least from a plane including the lower surface of the sealing member to beyond that of the uppermost surface of the sealing member, each of the outer leads comprising an upper electrical connecting surface located above the uppermost surface of the sealing member, and a lower electrical connecting surface located at the lower surface of the sealing member,

wherein each of the semiconductor packages is arranged to be mounted on the printed wiring board such that the uppermost surface of the sealing member faces the printed wiring board.

16. (New) The semiconductor device according to claim 14, wherein the upper electrical connecting surfaces of the outer leads lie outside an area over the upper surface of the sealing member.

17. (New) The semiconductor device according to claim 14, wherein the sealing member has four sides surrounded by the outer leads.

18. (New) The semiconductor device according to claims 14, wherein the outer leads are formed in an L-shape.

19. (New) The semiconductor device according to claim 14, further comprising a cooling fin arranged to be provided on an exposed surface of the die pad.

20. (New) The semiconductor device according to claim 14, wherein each of the semiconductor package is arranged to be mounted on the printed wiring board such that the uppermost surface of the sealing member faces that of another semiconductor package through the printed wiring board.